AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

Listing of Claims:

Claims 1.-16. (Cancelled).

17. (Currently Amended) A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) preparing a set of first photomasks including one or more resist masks;

(b) transferring each pattern of said plurality of first photomasks onto a second photomask by reduced projection exposure; and

(c) transferring the pattern on said second photomask onto a semiconductor wafer by reduced projection exposure,

wherein said set of first photomasks include a least one photomask having an alignment mark made of organic film having a light-shielding property or a light-reducing property to exposure light.

18. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 17, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said second photomask.

19. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 17, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in the integrated circuit pattern region of said second photomask.

20. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 17, wherein both of a metal pattern having a light-shielding property to exposure light and an organic film pattern having a light-shielding property or a light-reducing property to exposure light are arranged in an integrated circuit pattern region of said second photomask.

21. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 20, further comprising the step of removing said organic film pattern of said second photomask.

22. (Currently Amended) A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) preparing a plurality of IP masks, at least one of which is made of a resist mask,

(b) transferring each pattern of said plurality of IP masks onto a product mask by reduced projection exposure;

(c) transferring a pattern of said product mask onto a semiconductor wafer by reduced projection exposure,

wherein said plurality of IP masks include at least one IP mask having an alignment mark made of organic film having a light-shielding property or a light-reducing property to exposure light.

23. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 22, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said product mask.

24. (Currently Amended) The method of manufacturing a semiconductor integrated circuit device according to claim 22, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in a ~~an~~ light-shielding pattern of the integrated circuit pattern region of said product mask.

25. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 22, wherein both of a metal pattern having a light-shielding property to exposure light and an organic film pattern having a light-shielding property or a light-reducing property to exposure light are arranged in an integrated circuit pattern region of said product mask.

26. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 25, further comprising the step of removing said organic film pattern of said product mask.

27. (Currently Amended) A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) preparing ~~an~~ at least one IP mask made of a resist mask, which is a photomask used in transfer of a memory mat or an aggregate of the memory mats;

(b) transferring the pattern of said IP mask onto a product mask by reduced projection exposure; and

(c) transferring the pattern of said product mask onto a semiconductor wafer by the reduced projection exposure,

wherein said at least one IP mask has an alignment mark made of organic film having a light-shielding property or a light-reducing property to exposure light.

28. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 27, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said product mask.

29. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 27, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in an integrated circuit pattern region of said product mask.

30. (Currently Amended) A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) preparing a first IP mask made of a resist mask, which is a photomask used in ~~an~~ a transfer of a memory mat or an aggregate of the memory mats;

(b) preparing a second IP mask made of a resist mask, which is a photomask used in ~~an~~ a transfer of a peripheral circuit region of said memory mat;

(c) transferring the patterns of said first and second IP masks onto a product mask by reduced projection exposure; and

(d) transferring the pattern of said product mask onto a semiconductor wafer by reduced projection exposure,

wherein said first IP mask and said second IP mask have an alignment mask made of organic film having a light-shielding property or a light-reducing property to exposure light.

31. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 30, wherein a metal pattern having a light-shielding property to exposure light is arranged in an integrated circuit pattern region of said product photomask.

32. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 30, wherein an organic film pattern having a light-shielding property or a light-reducing property to exposure light is arranged in the integrated circuit pattern region of said product mask.

33. (New) The method of manufacturing a semiconductor integrated circuit device according to claim 17, wherein all of the set of first photomasks have an alignment mark made of organic film having a light-shielding property or a light-reducing property to exposure light.

34. (New) The method of manufacturing a semiconductor integrated circuit device according to claim 22, wherein all of the set of IP masks have an alignment mark made of organic film having a light-shielding property or a light-reducing property to exposure light.

35. (New) The method of manufacturing a semiconductor integrated circuit device according to claim 28, wherein there are a plurality of said IP masks, and all of said plurality of IP masks have an alignment mark made of organic film having a light-shielding property or a light-reducing property to exposure light.